Interface engineering in high-k gate stacks for nanoelectronic devices

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The interfaces between metal, oxide and semiconductor are very critical for the application of metal/oxide thin films, including gate dielectrics and ferroelectric transistors. Much research has focused on understanding and exploiting the properties of novel metal/oxide/semiconductor interfaces to fulfill the stringent requirements for these and other applications. With the alternative high-k gate dielectrics are expected to replace current SiO_2 gate oxide for the continued scaling of metal-oxide-semiconductor field-effect transistors (MOSFET), there is an immense interest in replacing conventional poly-Si gate with metal gates because of the serious problems related to poly-Si gate depletion and high gate resistance. However, the possible atomic bonds of metal-metal or metal-oxygen at metal gate/oxide gate dielectric interface are quit different from conventional silicon-oxygen bond at poly-Si-SiO_2 interface. How these bonds affect the band alignment at the metal/high-k oxide interface is am important issue for the implementation of this gate stack in nanoelectronic devices. In this talk, I will present the band alignment studies of high-k gate stacks by photoemission study and first-principle calculation. The Schottky-barrier heights for the Ni and ZrO_2 (HfO_2) interfaces have been determined by means of x-ray photoemission spectroscopy (XPS). Depending on the interface treatment, the band alignment could be tuned. First-principles calculations for model interfaces provide a microscopic explanation of such variation. The results show that the band alignment at metal/high-k/semiconductor could be engineered through the interface structure-control.